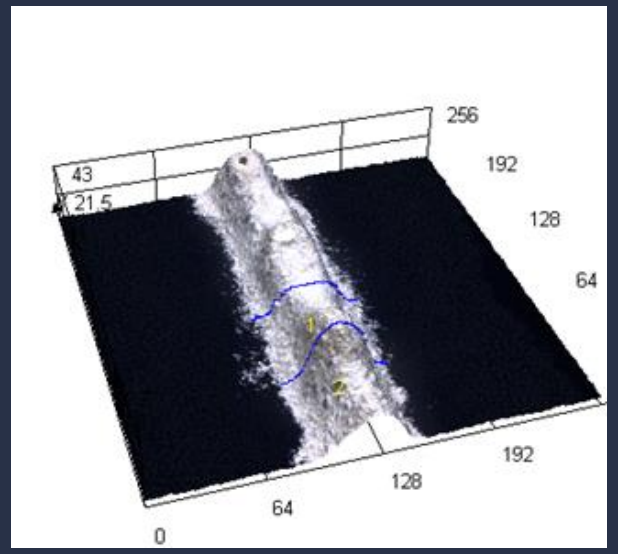
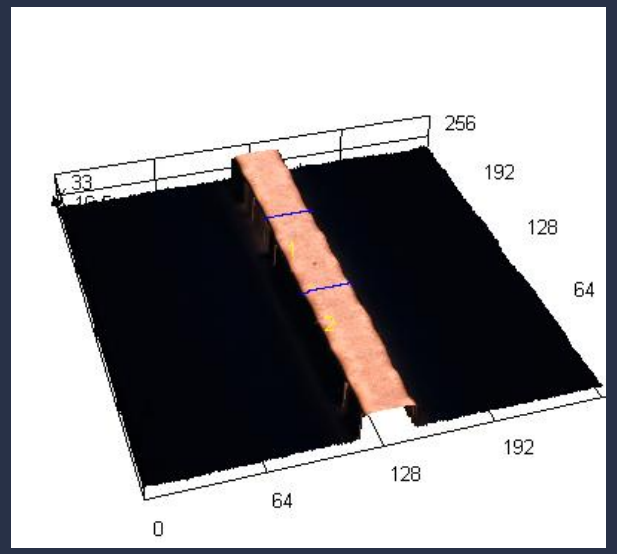
Project Ameliz: Patterning Techniques for Copper Electroplated Metallization on Heterojunction Cells





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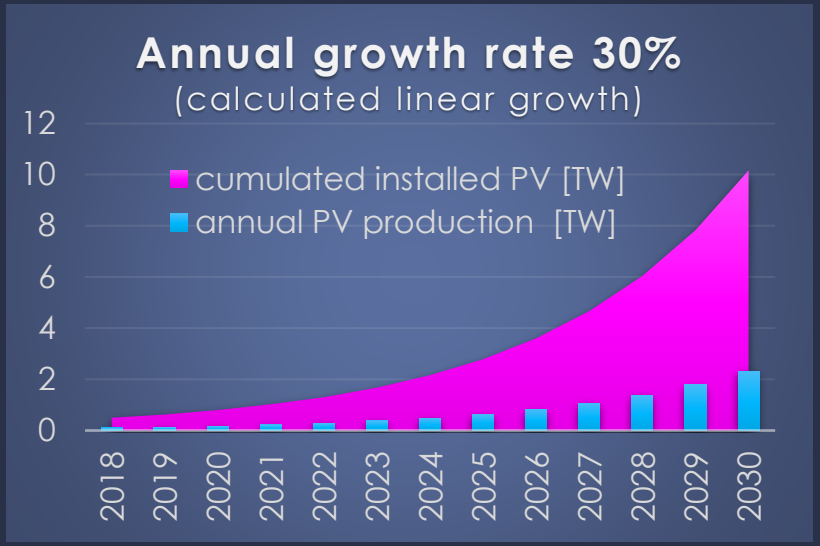
There might be not enough silver…
for all the solar cells needed in the future

- PV production is supposed to grow to terawatt levels to enable energy transition to 100% renewables. Leading scientists postulate ~2 TW p.a. already for 2030. [1,2]
- For todays annual production of around 100 GW more than **2000 metric tons of silver** are consumed. *
  10% of the annual silver supply have been consumed for the PV sector in 2019 (2800 tons).[3]
- **Silver price has increased by >50% in the last months.**
- Paste consumption for bifacial heterojunction cells with busbars for interconnection with soldered ribbons is particularly high, 300 mg/cell.



10 TW total

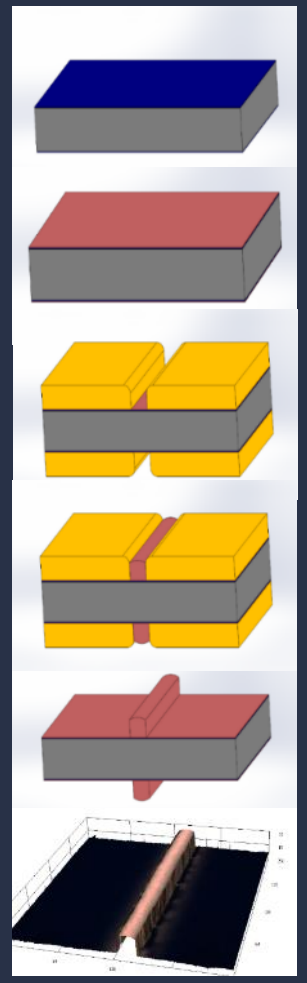
2 TW p.a.

* Assumed 100 mg silver and 5 W per cell and 100 GW annual production

[1] N. Haegel et al., Science, 2019
[2] P. Verlinden, HJT Workshop, 2019
[3] World Silver Survey 2020, silverinstitute.org

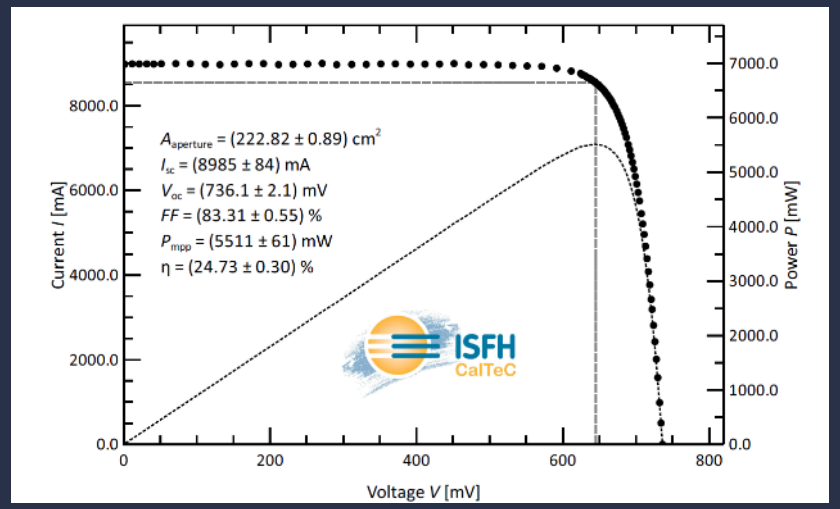
CSEM baseline process for heterojunction cells

- Precursor with TCO
- PVD seed layer stack
- Hotmelt inkjet mask
- Copper plating
- Mask removal
- Seed layer etchback



Width [µm]	Height [µm]
24.170	24.882

- Line resistivity: 2 µΩ·cm
- Contact resistivity: < 1 mΩ·cm²
- Adhesion: peel force 4 – 5 N/mm (180° peel test on soldered ribbons)
- Efficiency: > 24.7% on an industrial precursor, monofacial, 4BB



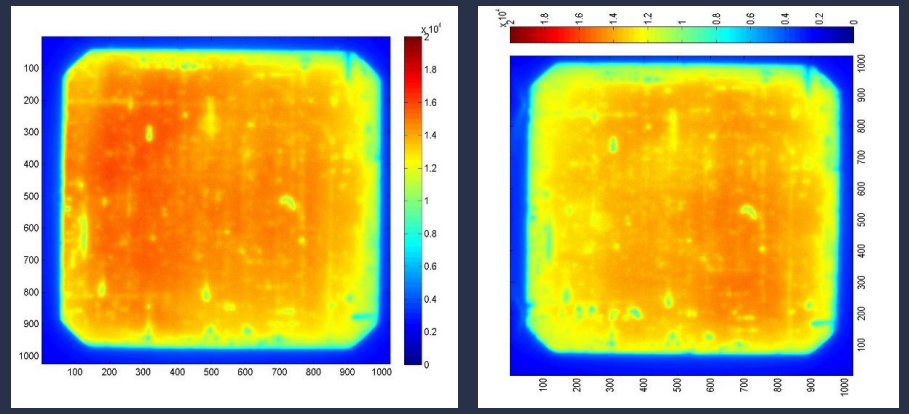
- Excellent module stability:
  1-cell GG modules, 4BB with soldered ribbons:
  tested until > 500 TC (-2.3%) and > 3000 h DH (-2.8%)
- SmartWire Interconnection:
  stability exceeds 3x the IEC 61215 norm *

* **Busbar-less cells with pure copper seed layer**

Copper sputtered directly on heterojunction cell precursors

- TCOs are excellent barriers against copper diffusion. [1,2]
- Pure copper seed layer sputtered directly on HJT cell precursors with ITO
  Annealing at 190°C, 1h
  Seed layer etching and PL measurement
  No impact on PL intensity
- Test repeated on precursors with IWO
  Annealing with sputtered copper 1h at 190°C
  No impact on PL intensity

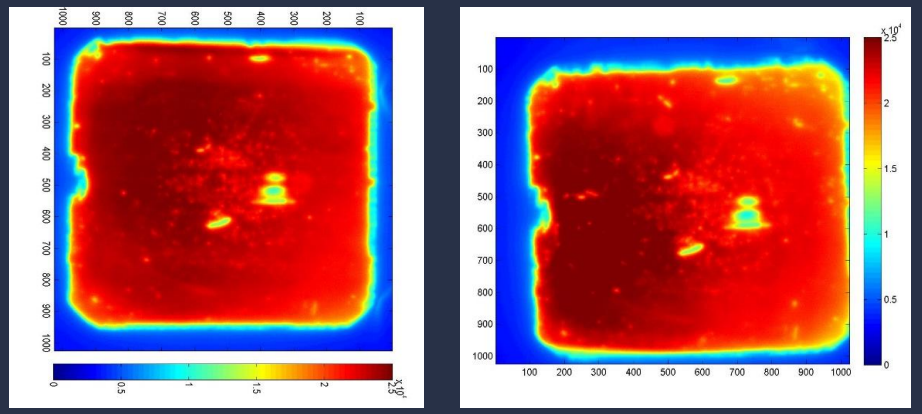
N-side
fully covered with ITO



Before PVD

After annealing with copper on ITO

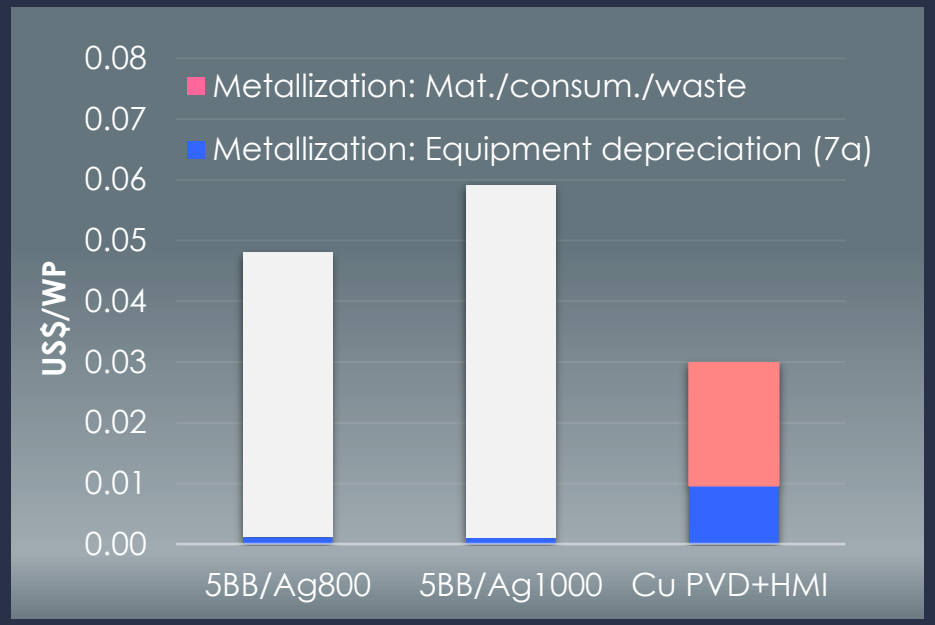
P-side
ITO deposited with mask, edges only a-Si. ITO thickness: 50 nm



[1] C. Liu et al., "ITO as Diffusion Barrier Between Si and Cu", ECS, 2005
[2] J. Yu et al., "Tungsten doped indium oxide film: Ready for bifacial copper metallization on silicon hetrojunction solar cell", Solmat, 2016

Process cost

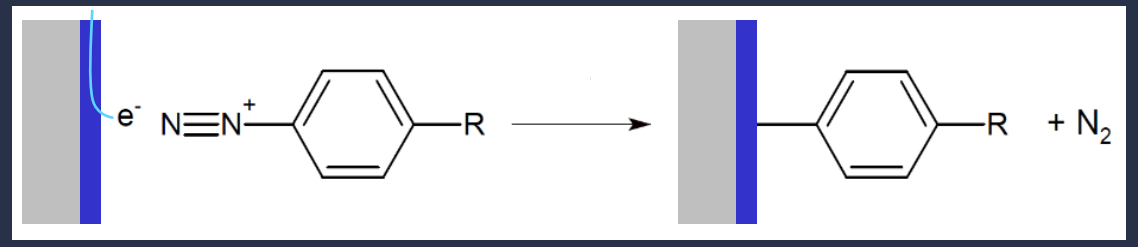
- Cost advantage to screen printing:
  - HJT cells for interconnection with soldered ribbons: high paste consumption, increasing silver paste price
- Baseline plating process
  - High capex: PVD, inkjet printer, plating line
  - Organic mask: high material cost
- Development focused on the replacement for the PVD seed layer and on alternative masking materials. Project Ameliz: **A**dvanced **ME**ta**LIZ**ation Strategies for Heterojunction Solar Cells



Calculated with **300 mg paste laydown** for a bifacial HJT cell for ribbon interconnection. For silver paste price 800 and 1000 US$/kg.

Electrografted copper seed layer on ITO [1]

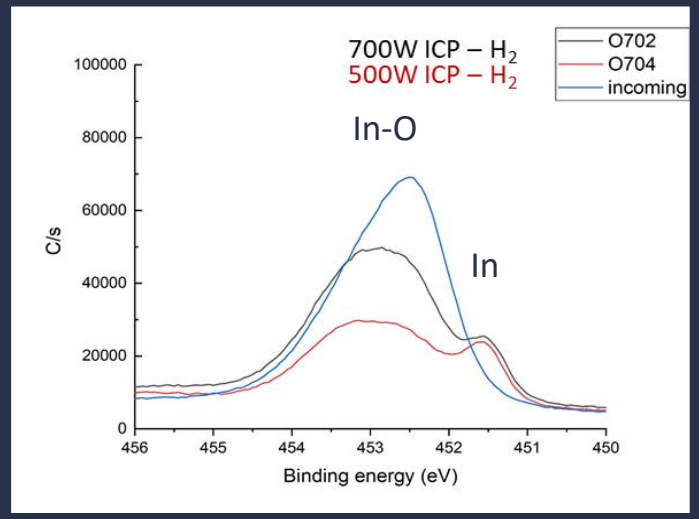
- An electrolyte containing copper ions and a benzo-diazonium compound with good complexing properties for copper is used. Copper ions and the benzodiazonium salt are electrochemically reduced. The challenge is to deposit copper without passivating the surface by the organic compound.
- 300 nm thick, well adherent, copper-rich layers have been obtained on small patterned samples with polished surface.
- Next step: application on bigger cell precursors with textured surface, measurement of contact resistivity.



[1] P.H. Haumesser et al., Material Research Society, 2004

ITO reduction

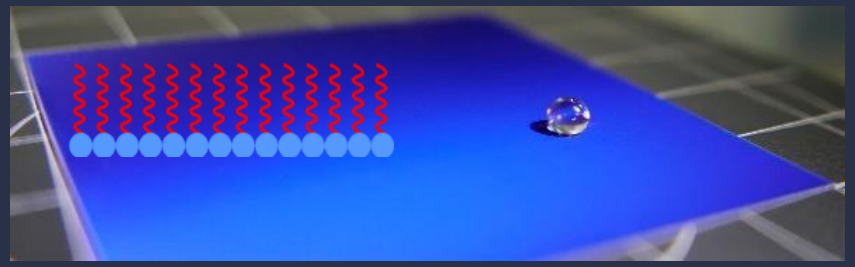
- The topmost ITO layer is reduced by hydrogen plasma to promote adhesion of the subsequently electrodeposited metal layer.
- ITO reduction has been realized by inductively coupled plasma, confirmed by XPS and by lowered sheet resistance.
  A smooth indium layer was observed, without spheres as may happen on electrochemically reduced ITO.
  First tests with nickel layers plated on the reduced ITO indicate good adhesion.
- Optimization of the plasma parameters is ongoing to fully eliminate the remaining minor impact on cell passivation.



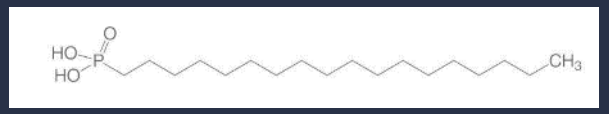
Cell precursor	Rsheet [Ω/sq]
As received	339
500W ICP-H2	156
700W ICP-H2	81

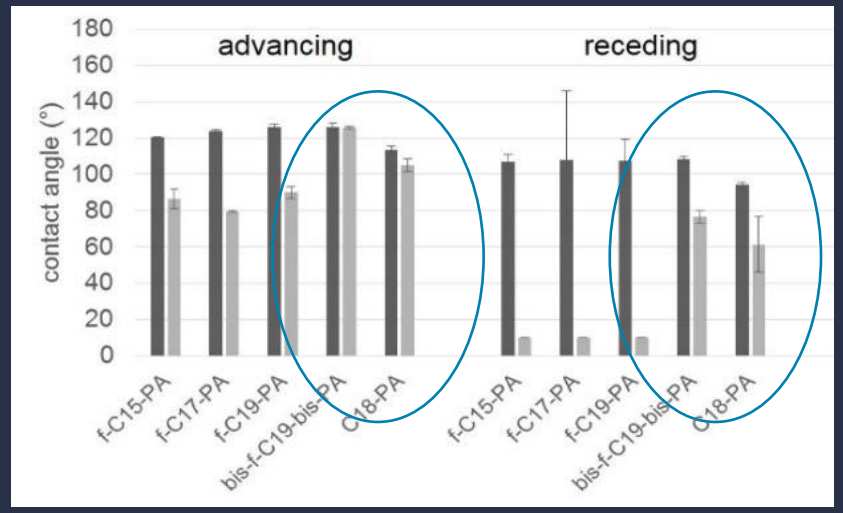
Self assembled monolayer as plating mask [1]

- Commercially available perfluorinated phosphonic acids and octadecyl phosphonic acid (C18-PA) were applied at first on polished silicon wafers with ITO. Highly hydrophobic layers are formed, the thickness ranging between 0.9 to 2.6 nm (measured by XRR). Accordingly the material amount consumed per one wafer side is very small and below 1 mg.
  Material consumption reduced by a factor of roughly 1000x compared to an organic mask.
- Resistance to highly acidic electrolytes has been tested by dynamic contact angle measurement and two molecules have been selected for application on textured precursors.
- Application on textured M2 wafers by spraying.



C18-PA



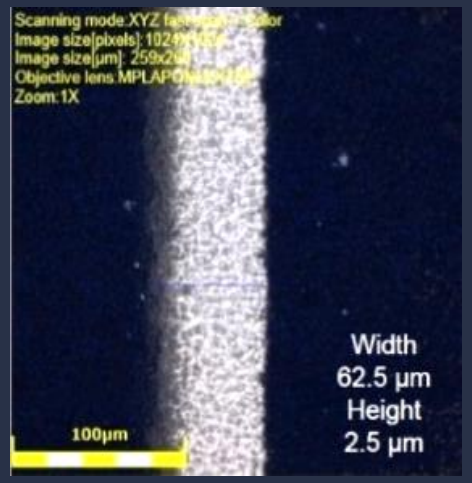


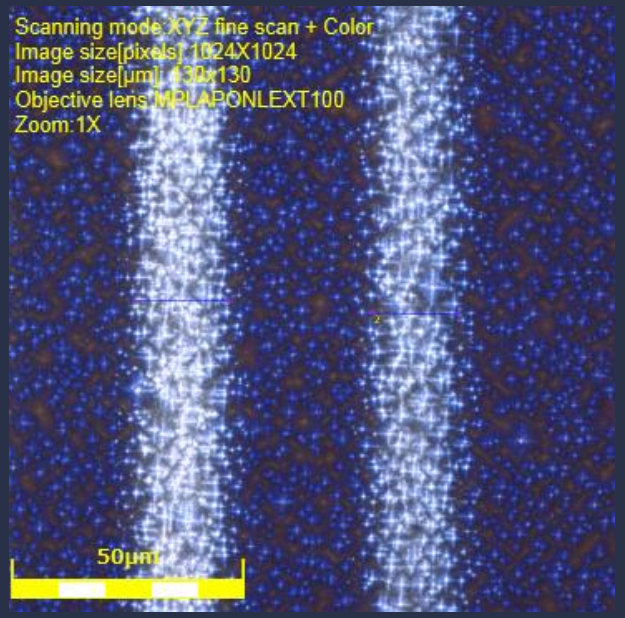
Dynamic contact angle measurement before (dark grey) and after immersion (light grey bars) during 10 min in highly acidic copper electrolyte

[1] G. Andreatta et al., Thin Solid Films, 2019

Plating test with SAM mask

- SAM coated samples have been patterned with oxygen plasma using a hard mask. 62 µm lines were obtained after plating of a thin nickel layer, residual ghost plating is observed.
- With improved patterning 20 µm lines have been realized.
- Next step: plating test in acidic copper electrolyte on patterned M2 precursors

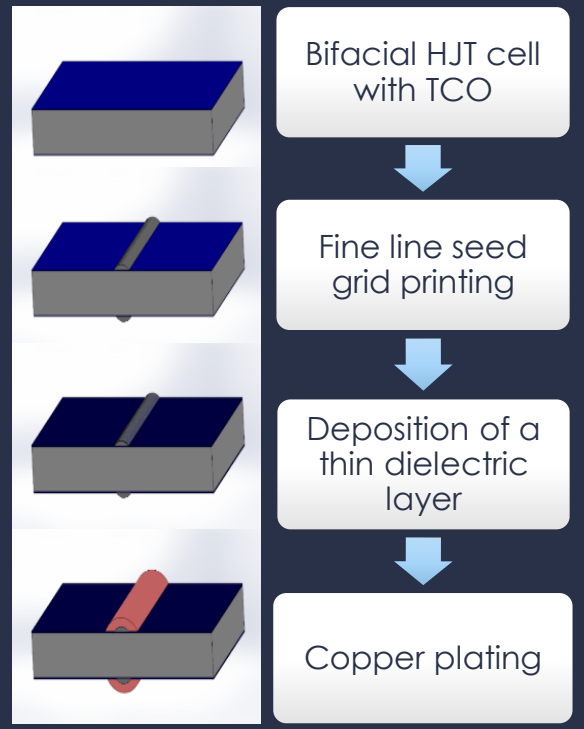


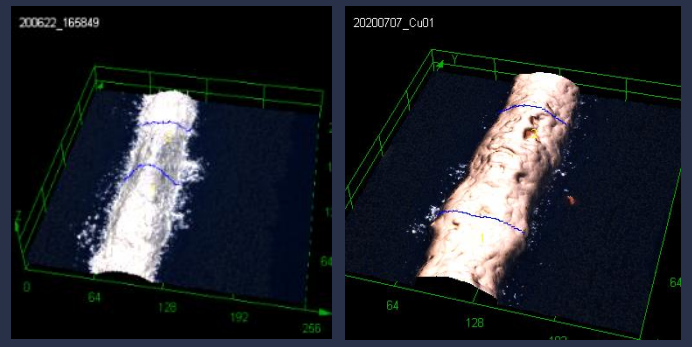


Line width 20 µm
(after nickel plating)

Printed seed grid and a thin dielectric layer as plating mask [1]

- Short process sequence
- With silicon oxide layers deposited by PECVD minor ghost plating has been observed in standard acidic copper electrolytes.
- First cells fabricated with standard screen–printed grid with silver paste and an ALD-AlOx layer 8nm.
  Parasitic plating on fingerprints.
  Lower Jsc after plating.
  Goal: plating on very fine lines, the required conductivity will be provided by electrodeposited copper





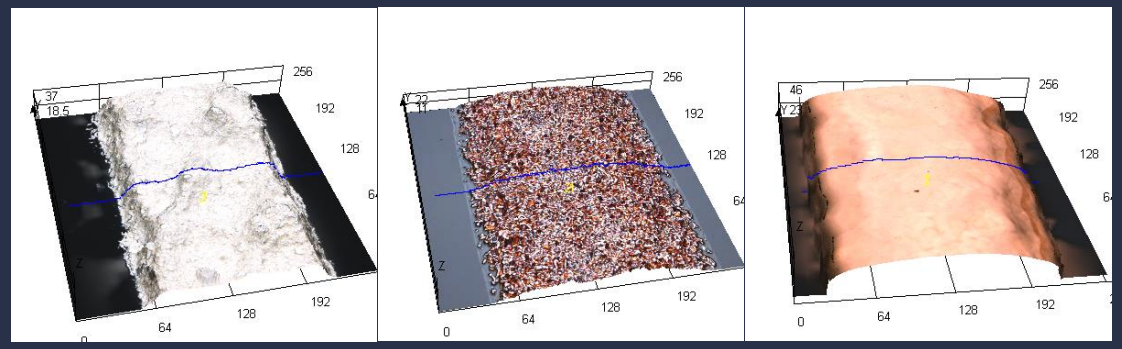
[1] C. Ballif, EP 2 489 076, 2010

Printed seed grid and a thin dielectric layer as plating mask: copper paste

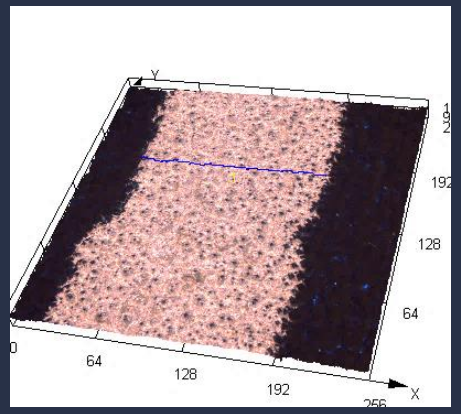
- Two types of copper paste tested on textured precursors.
- Specific resistivity of low temperature silver paste, copper paste and electrodeposited copper on copper paste:

Line	Cross section [µm²]	Resistance [Ω]	Specific resistivity [µΩ · cm]
Ag paste (curing at 200°C)	2925	0.12	4.0
Cu paste (curing at 200°C)	1880	1.24	27.4
Cu plated on Cu paste	5480	0.04	2.8
Cu plated, paste area subtracted	3600	0.04	1.8

Measured on 200 µm lines, line length 1.1 mm, printed on glass.



Screen opening 40 µm



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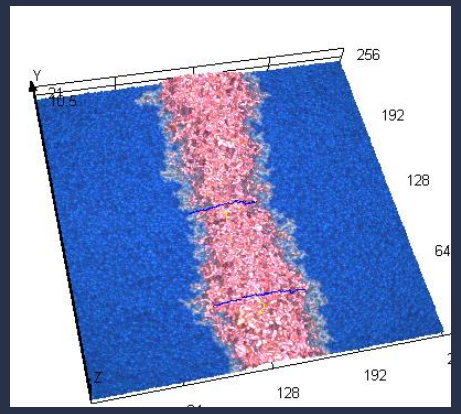

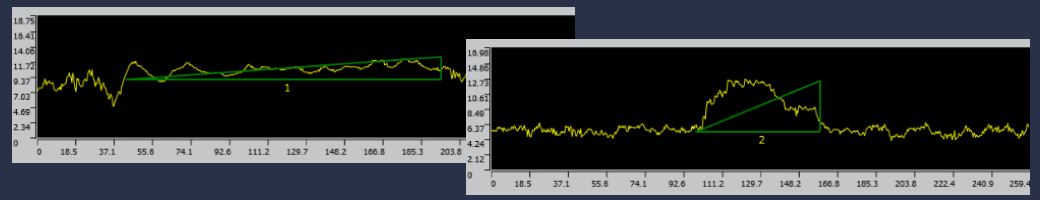

- No impact on PL signal after 1 h annealing of printed copper paste at 200°C
  Tested on precursors with ITO and IWO
- Contact resistivity 3.5 mΩ·cm²

Summary

- Growing need for replacement of silver because of increasing increasing PV production volumes and increasing silver price
- Reliable plating process with PVD seed layer and hotmelt inkjet patterning available, cost reduction and reduction of material consumption to continue.
- Electrografting of a copper seed layer and ITO reduction for improved adhesion demonstrated.
- Application of SAMs by spraying on industrial size textured wafers and patterning for 20-micron lines demonstrated.
- First cells with printed seed grid and a dielectric layer fabricated.
  The possibility to use copper paste as seed-grid makes the process even more cost competitive to standard silver screen-printing.
- Heterojunction cells are resistant against copper ingress.

Acknowledgment
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Thank you very much for your attention!

Q&A

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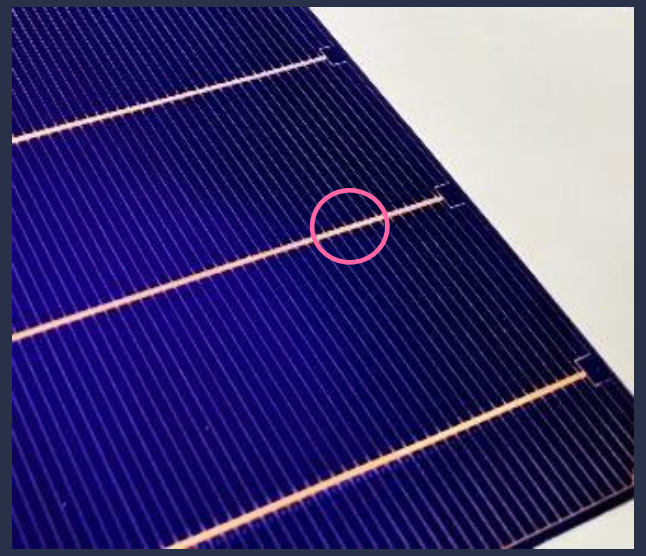
Supporting information: electromigration

- Electromigration has been observed on integrated circuits, on aluminum and on copper
- The values for current density per track cross section, at which electromigration can occur are:
  ~0.5 MA/cm² for aluminum and
  ~1 MA /cm² for copper [1,2]
- Current density per finger cross section on a solar cell:
  ~15 kA/cm² *
  This is two orders of magnitude lower than on ICs and therefore electromigration is not expected to happen on solar cells.



* Calculation for:
4 BBs, 10 A per cell, 80 fingers
Finger dimensions: 10 µm x 10 µm

[1] https://en.wikipedia.org/wiki/Electromigration
[2] J. Lienig, M. Thiele, ISPD, 2018